WHAT IS CLAIMED IS:

1. A liquid crystal display (LCD) comprising:

a timing controller for receiving external image data, and outputting a vertical sync start signal based on a data-enable signal having an irregular output interval to control output of the image data, the vertical sync start signal having a generation interval associated with a blank interval of the data-enable signal;

a data driver for converting the image data and outputting the same;

a gate driver for sequentially applying both a first gate-on voltage and a second gate-on voltage to a same gate line, wherein the first gate-on voltage is to drive a previous line being most adjacent to and having the same polarity as a present line, and the second gate-on voltage is to drive the present line; and

an LCD panel being first charged with the first gate-on voltage supplied from the gate driver, and second charged with the second gate-on voltage, wherein the LCD panel displays the image data received from the data driver during the second charging.

2. The LCD as claimed in claim 1, wherein the one vertical sync start signal comprises a signal for generating the first gate-on voltage and a signal for generating the second gate-on voltage.

3. The LCD as claimed in claim 1, wherein the timing controller comprises:

an internal data-enable converter for receiving the data-enable signal having an irregular output interval, and outputting an internal data-enable signal after being shifted by a predetermined number of lines;

a counter for counting data-enable signals applied to the internal data-enable converter to output a first switching signal and a second switching signal;

a control signal generator for receiving the internal data-enable signal shifted by the predetermined number of lines to output a control signal for driving the LCD panel;

a first switch having one input path and a plurality of output paths, for determining an output path of the image data signal based on the first switching signal;

a memory section having a plurality of memories for respectively storing image data received via the first switch, and outputting the stored image data when the image data of a next line is applied to the timing controller; and

a second switch having a plurality of input paths and one output path, for determining an input path of the image data received from the memory section based on the second switching signal, and outputting the image data to the data driver.

4. The LCD as claimed in claim 3, wherein the predetermined number of lines is at least one.

5. The LCD as claimed in claim 3, wherein the internal data-enable signal is generated in synchronization with the input data-enable signal shifted by a predetermined number of lines, the internal data-enable signal having the same polarity as the input data-enable signal.

6. The LCD as claimed in claim 3, wherein the memory comprises a line memory.

7. An apparatus for driving an LCD, which includes an LCD panel having a plurality of data lines and gate lines, and which charges a specific pixel by (1) first charging the data of a pixel adjacent to the specific pixel and having the same polarity as the specific pixel to change the polarity of the corresponding pixel, and (2) second, charging the data of the specific pixel,

the LCD comprising:

a timing controller for receiving external image data, and outputting one vertical sync start signal based on a data-enable signal having an irregular output interval to control the output of the image data, the one vertical sync start signal having a generation interval associated with a blank interval of the data-enable signal;

a data driver for converting the image data and outputting the converted image data to one of the data lines of the LCD panel; and

a gate driver for applying a first gate-on voltage in a first charging to the gate line of the LCD panel, and a second gate-on voltage in a second charging to the gate line, based on the vertical sync start signal, and controlling display of the converted image data supplied from the data driver during the second charging, wherein the first gate-on voltage drives a previous line being most adjacent to and having the same polarity as a present line, and the second gate-on voltage drives the present line.

8. The apparatus as claimed in claim 7, wherein the one vertical sync start signal comprises a signal for generating the first gate-on voltage and a signal for generating the second gate-on voltage.

9. The apparatus as claimed in claim 7, wherein the timing controller comprises:

an internal data-enable converter for receiving the data-enable signal having an irregular output interval, and outputting an internal data-enable signal shifted by a predetermined number of lines;

a counter for counting the data-enable signals applied to the internal data-enable converter to output a first switching signal and a second switching signal;

a control signal generator for receiving the internal data-enable signal shifted by the predetermined number of lines to output a control signal for driving the LCD panel;

a first switch having one input path and a plurality of output paths, for determining an output path of the image data signal based on the first switching signal;

a memory section having a plurality of memories for respectively storing image data received via the first switch, and outputting the stored image data as the image data of a next line is applied to the timing controller; and

a second switch having a plurality of input paths and one output path, for determining an input path of the image data received from the memory section based on the second switching signal, and outputting the image data to the data driver.

10. The apparatus as claimed in claim 9, wherein the predetermined number of lines is at least one.

11. The apparatus as claimed in claim 9, wherein the internal data-enable signal is generated in synchronization with the input data-enable signal shifted by a

predetermined number of lines, the internal data-enable signal having the same polarity as the input data-enable signal.

12. The apparatus as claimed in claim 9, wherein the memory comprises a line memory.

13. A method for driving an LCD that includes an LCD panel having a plurality of data lines and gate lines, which charges a specific pixel by (1) first charging the data of an pixel adjacent to the specific pixel and having the same polarity as the specific pixel to change the polarity of the corresponding pixel, and (2) second charging the data of the specific pixel,

the method comprising:

(a) receiving image data from an external image signal source and a data-enable signal for controlling output of the image data;

(b) checking whether the data-enable signal has been received, sequentially recording the image data on a predetermined number of built-in memories upon receiving the data-enable signal, sequentially extracting the recorded image data, and generating an internal data-enable signal upon extraction of the image data to output a vertical sync start signal having a generation interval associated with a blank interval of the data-enable signal;

(c) applying a voltage corresponding to the image data to the data lines; and

(d) sequentially applying both a first gate-on voltage and a second gate-on voltage based on the vertical sync start signal, wherein the first gate-on voltage drives a

previous line being most adjacent to and having the same polarity as the present line, and the second gate-on voltage drives the present line.

14. The method as claimed in claim 13, wherein the built-in memories comprise a line memory.

15. The method as claimed in claim 13, wherein the vertical sync start signal comprises a signal for generating the first gate-on voltage and a signal for generating the second gate-on voltage.

16. The method as claimed in claim 13, wherein the predetermined number is at least one.

17. The method as claimed in claim 16, wherein the internal data-enable signal is generated in synchronization with the input data-enable signal shifted by a predetermined number of lines, the internal data-enable signal having the same polarity as the input data-enable signal.

18. The method as claimed in claim 13, wherein the output of the vertical sync start signal when sequentially extracting the data in step (b) comprises:

(b-11) initializing a line count value and an internal flag;

(b-12) checking whether the data-enable signal is present;

(b-13) increasing the line count value by one and checking whether the updated

line count value is greater than a first number of lines, which is the number of gate lines plus one, when the data-enable signal exists in step (b-12);

(b-14) returning to step (b-12) when the updated line count value is equal to or less than the first number of lines, and generating a memory extraction flag signal to extract the data when the updated line count value is greater than the first number of lines;

(b-15) checking whether the updated line count value is equal to the number of gate lines, and if not, returning to step (b-12);

(b-16) generating an internal flag signal and increasing an internal flag count value by one, when the updated line count value is equal to the number of gate lines in step (b-15) or when the data-enable signal does not exist in step (b-12); and

(b-17) comparing the updated interval flag count value with the first number of lines, ending the flow of the method when the internal flag count value is greater than the first number of lines, and returning to step (b-16) when the internal flag count value is equal to or less than the first number of lines.

19. The method as claimed in claim 13, wherein the output of the vertical sync start signal when recording the data in step (b) comprises:

(b-21) initializing a line count value;

(b-22) checking whether the data-enable signal is present, ending the flow of the method when the data-enable signal does not exist, and increasing the line count value by one when the data-enable signal exists;

(b-23) generating a memory-recording flag signal to record the data; and

(b-24) checking whether the updated line count value in step (b-22) is equal to the number of vertically arranged gate lines, ending the flow of the method when the updated line count value is equal to the number of gate lines, and returning to step (b-22) when the updated line count value is not equal to the number of gate lines.

20. A pre-charging method in which a normal LCD image display is provided based on irregular-interval effective data, comprising:

providing one vertical sync start signal based on a data-enable signal having an irregular output interval to control output of the image data, the one vertical start signal having a generation interval associated with a blank interval of the data-enable signal

based on the one vertical start signal, applying a first gate-on voltage and a second gate-on voltage to a same present gate line, wherein the first gate-on voltage drives a previous line being most adjacent to and having the same polarity as a present line, and the second gate-on voltage drives the present line;

charging an LCD panel with the first gate-on voltage, and then with the second gate-on voltage.

21. A pre-charging method according to claim 20, wherein the LCD panel displays image data received during application of the second gate-on voltage.